Implementation of Negative Impedance Linearisation With CMOS Differential Amplifier

M Tanseer Ali, Ruiheng Wu, Predrag Rapajic and Peter Callaghan
University of Greenwich, School of Engineering,
Chatham Maritime, Medway, Kent,
ME4 4TB, UK

Abstract — **In this paper a promising linearization technique with negative impedance compensation has been implemented with a CMOS differential amplifier. The linearized amplifier achieves high gain accuracy (5% improved gain) and high linearity (IMD3 improved from 20.8dB to 24.5dB). The novel design technique is proposed here is potential for wireless RF and microwave application.**

Keywords - CMOS differential amplifier, linearization, RF feedback, negative impedance compensation;

I. INTRODUCTION

Wireless technology adoptions exploding very rapidly in recent years. The high demand for inexpensive, portable, high data rate wireless products in mass consumer markets is driving the semiconductor industry towards total integration and implementation of a complete transceiver on a system on chip (SoC) [1-7]. At high frequencies the cost of these amplifiers grows rapidly. Designing broadband amplifiers for digital signal transmission presents a tradeoff between efficient amplifiers that create distortion or unnecessarily large and inefficient amplifiers without distortion.[8] Therefore in current CMOS technology the design process trapped in to a trade off cycle.[9] One solution to break this cycle is to use a linearization technique which does not compensate the gain or bandwidth, if this constrained link is broken, and then the CMOS analogue circuit could achieve more design flexibility.

In this paper, an effective and practical technique for designing CMOS RF differential amplifier with excellent linearity, wide bandwidth and high gain accuracy will be investigated; the amplifier has been developed utilizing a new technique based on a negative impedance distortion correction method [10-13]. In spite of the advantages, the RF feedback topology the output signal still inherits some distortions as the main amplifier used for the forward gain path does not reacts as ideal assumptions which is also demonstrated with the analytical calculations in [10]; hence the an additional linearization technique is required to devise in order to neutralize the effects of nonlinearity of RF feedback topology. The proposed linearization method has been realized with BJT differential amplifier in [10, 14], the application of the linearization technique in CMOS two stage differential amplifier is novel.

The proposed linearization technique perform in two channel scheme, where the main amplifier provides the forward gain while the auxiliary amplifier utilized to realize the compensating negative impedance; hence both amplifier can be built around with similar specification minimizing complexity of the design. Following the expected gain accuracy and high linearity of the technique [10, 14], the linearized CMOS differential amplifier presented in this paper also improves the gain and linearity at the output compared with the amplifier without linearization.

In section II we start with an overview of the linearization technique with the negative impedance compensation. Section III presents the design technique of the linearized CMOS differential amplifier with linearization whilst section IV demonstrates the simulation results with discussion.

II. DISTORTION ANALYSIS AND LINEARIZATION

All amplifiers posses the property of distorting the signals they are required to amplify [15]. The existence of distortion is caused by nonlinearity of the amplifier. The harmonic content of the output from an amplifier gives a measure of the level of nonlinearity.

A. RF Feedbcak Topology

In this research the main methodology has been considered as Inverting Feed Back Amplifier where the main amplifier is commonly used as differential amplifier. The basic configuration of an Inverting amplifier could be considered as figure 1.

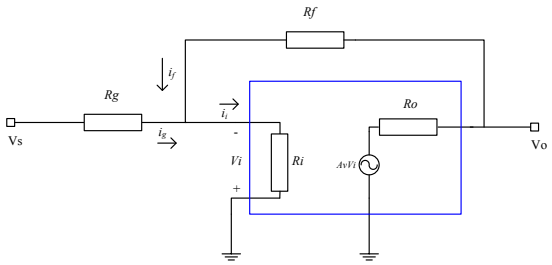

Figure 1. AC equivalent circuit of conventional Inverting Feed Back Amplifier

In practical amplifier, the input voltage of the main amplifier can be solved by nodal analysis, where non ideal open loop gain A is finite or nonlinear, considering $R_i \neq \infty$ and $R_o \neq 0$, the difference of ideal input current and non-ideal input current can be obtained as the distortion current.

$$\frac{V_O}{R_f} + \frac{V_O}{A}\left(\frac{1}{R_f} + \frac{1}{R_g}\right) = -\frac{V_S}{R_g} \quad (1)$$

B. *Negative Impedance Compensation*

The proposed linearization technique in [11, 13] has been developed by analyzing the distortion current at the input; and the linearity of the feedback amplifier can be improved by means of negative impedance (as shown in figure 2), which effectively neutralize the distortion current.

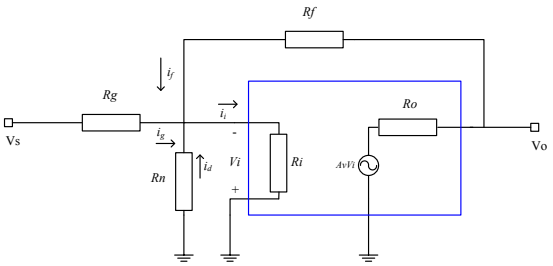

Figure 2. Negative Impedance Compensation

The compensating negative impedance can be considered as (3). As demonstrated in [11, 13], the distortion at the input of the amplifier can be minimized and hence the linearity can be improved.

$$R_n = -\left(R_g \,||\, R_f\right) \quad (2)$$

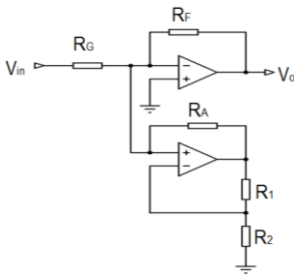

Figure 3. Complete Circuit with Linearisation

Ideally the negative impedance can be realized when the current travels from low voltage to higher voltage node, alternatively if the current drops with increasing voltage. For the differential amplifier design, the negative impedance compensation has been implemented with non-inverting amplifier configuration as shown in figure 3, where the input impedance from the input terminal will be realized as (3).

$$R_n = -R_A\left(\frac{R_2}{R_1}\right) \quad (3)$$

So the ratio R_2 / R_1 acts as the multiplying factor of Z to realize the input impedance. Now when the multiplying factor is set as unit, i.e. $R_2 = R_1$, then (3) yields as $R_n = -R_A$. Thus the negative impedance can be realized by means of non-inverting auxiliary amplifier.

III. Design of CMOS Differential Amplifier

To demonstrate the application of the proposed method with a CMOS technology, the differential amplifier [8, 16] has been employed along with biasing circuit and output stage as shown in figure 4. The auxiliary amplifier (MA1-MA6) has been built around the same structure as main amplifier (M1-M8).

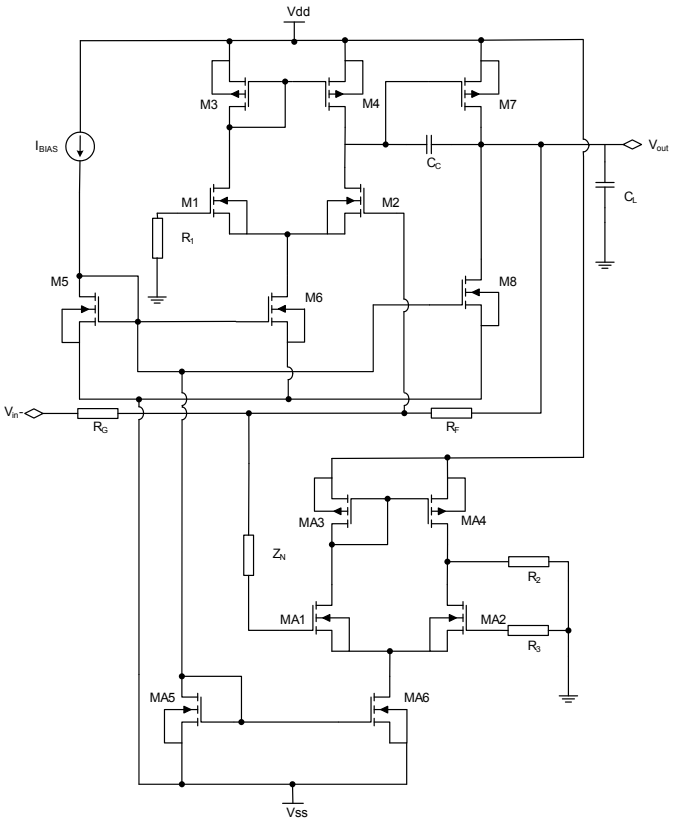

Figure 4. Complete CMOS Differential Amplifier With Linearization

Here the biasing circuit is not shown for sake of simplicity, although it is apparent that the single biasing circuit can drive both main and auxiliary amplifier, the load of the biasing circuit will increase, hence the parameters of the biasing circuit with the linearization method is modified to cope with the changed load.

In addition to that, the negative impedance realization also operates similar to positive feedback, as a result the gain improves, but as a trade-off the bandwidth decreases. The impact bandwidth due to negative compensation can be cancelled out by considering parallel resistive and capacitance as the compensating impedance, i.e. $Z_N = R_A || C_A$.

IV. Simulation Results

The pSpice simulations have been performed for the designed CMOS differential amplifier in figure 4 and the results are presented here.

A. DC Analysis

First the linearity of the circuit has been investigated by analyzing the DC transfer characteristics. For DC analysis, the amplifier has been considered with unit closed loop gain, i.e. R_G=R_F=2KΩ, and hence the compensation impedance has been used is R_N= -(R_G || R_F) = 1KΩ. The simulation result is shown in figure 5. For the designed CMOS differential amplifier the linear region is measured as the input range from -2 to +1.15, where as the negative impedance compensation provides range of -2.1 to +1.75 which is about 22% increment of the range.

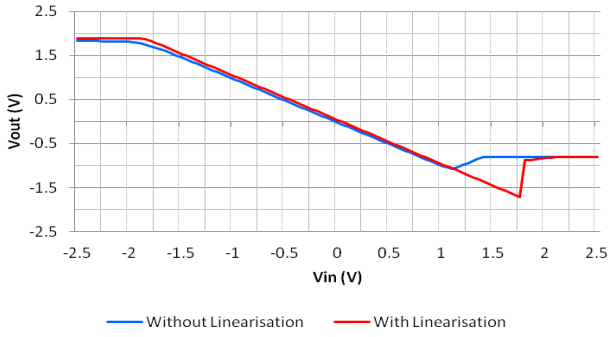

Figure 5. DC Transfer characteristics of CMOS Differential Amplifier (With and Without Linearization)

B. AC Analysis

The AC analysis is helpful for demonstrating the impact on gain and bandwidth for the proposed linearization technique. In this context the closed loop gain has been considered to be - 4, i.e. R_G=500Ω and R_F=2KΩ; hence the compensation impedance from the theoretical calculation from (2) suggests the value as R_N=400Ω. For the designed amplifier, the optimum value of R_N is found to be 380 Ω for. And the optimal value for C_N is considered to be 0.82P.

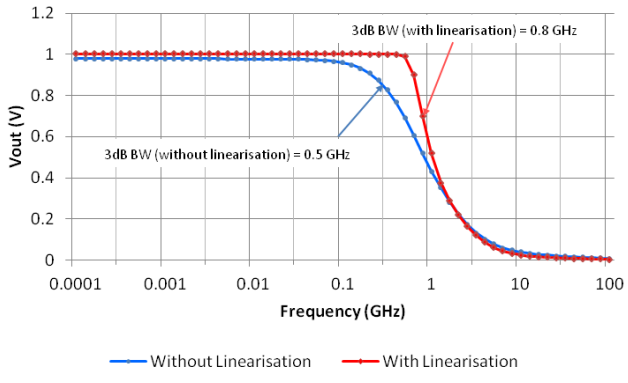

Figure 6. AC Analysis of CMOS Differential Amplifier (With and Without Linearization)

As shown in figure 6, the AC analysis has been carried out with and without linearization with 0.25V AC input signal. The circuit demonstrates the increase in closed loop gain (9% improved) by implementing the linearization technique. From the AC circuit simulation the 3dB bandwidth for the linearized amplifier has been obtained as 0.8 GHz, while the original amplifier had 3dB bandwidth of 0.5 GHz.

C. Two Tone Analysis

For the measurement of the level of distortion for the designed amplifier; a two tone test with f_1=1MHz and f_2=1.001MHz has been carried out with the circuit. Above simulation results, figure 7, proves that the gain has been improved with high linearity (IMD3 improved from 20.8dB to 24.5dB) using the proposed method.

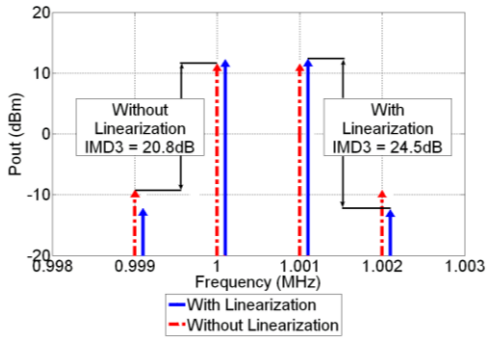

Figure 7. Example of a figure caption. (figure caption)

V. Conclusion

In this paper the differential amplifier design steps are followed with MOSFET technologies. The main methodology focused here, which is RF feedback topology, is widely used with differential amplifiers. The proposed linearization method by means of negative impedance compensation has been implemented to achieve high linearity.

From the simulation results it is evident that the designed CMOS differential amplifier demonstrates high linearity. All different analysis, DC, AC, single-tone excitation and two-tone excitation provide similar improved level of linearity. The main features of the linearization technique can be summarized into following advantages.

First, the main and auxiliary amplifiers can be the same design as CMOS differential amplifier developed in this paper follows same basic structure. For the same reason, the method differs from the traditional pre-distortion and feed-forward techniques in that a high precision auxiliary amplifier was not necessary. Finally this technique can be suitable for linearizing amplifiers with low open-loop gain, which is appropriate for RF/microwave applications as the differential amplifier discussed in this paper perform efficiently up to 0.8GHz bandwidth. In addition to that, high linearity and high gain accuracy has been achieved using the negative impedance linearization method.

REFERENCES

[1] A. Rofougaran, G. Chang, J. J. Rael, J. Y. C. Chang, M. Rofougaran, P. J. Chang, et al., "A single-chip 900-MHz spread-spectrum wireless transceiver in 1-μm CMOS. I. Architecture and transmitter design," Solid-State Circuits, IEEE Journal of, vol. 33, pp. 515-534, 1998.

[2] S. Raman, "Towards wireless single chip systems: challenges for RF integration in SoC," in Wireless Communication Technology, 2003. IEEE Topical Conference on, 2003, pp. 224-226.

[3] S. Signell, D. Rodriguez de Llera Gonzalez, and M. Ismail, "Radio design for future wireless soc platforms- an overview," in Norchip Conference, 2004. Proceedings, 2004, pp. 277-280.

[4] D. Su, "Challenges in Designing Low-Power CMOS Wireless Systems-on-a-Chip," in Custom Integrated Circuits Conference, 2006. CICC '06. IEEE, 2006, pp. 113-120.

[5] P. T. M. van Zeijl, "Wireless transceiver design for SoC and SDR," in Radio and Wireless Symposium, 2008 IEEE, 2008, pp. 807-810.

[6] G. Dan and F. Yaoxian, "A fully integrated SoC for large scale wireless sensor networks in 0.18µm CMOS," in Wireless Sensor Network, 2010. IET-WSN. IET International Conference on, 2010, pp. 90-94.

[7] Y. Ruan and W. Yao, "Design and Implementation of a SoC-Based Single Chip Radio Transceiver," in Wireless Communications, Networking and Mobile Computing (WiCOM), 2011 7th International Conference on, 2011, pp. 1-4.

[8] R. J. Baker, H. W. Li, and D. E. Boyce, CMOS circuit design, layout, and simulation. New York: IEEE Press, 1998.

[9] B. Razavi, "CMOS technology characterization for analog and RF design," Solid-State Circuits, IEEE Journal of, vol. 34, pp. 268-276, 1999.

[10] R. Wu, F. J. Lidgey, and K. Hayatelh,, "Design of amplifiers with high gain accuracy and high linearity," presented at the IEEE International Midwest Symposium on Circuits and Systems, Montreal, Canada, 5-8 Aug. 2007.

[11] R. Wu, F. J. Lidgey, K. Hayatelh and B. L. Hart, "Differential Amplifier With Improved Gain-Accuracy and Linearity," International Journal of Circuit Theory And Application, vol. 38, pp. 829-844, October 2010.

[12] R. Wu, "Design of Wide Bandwidth High Linearity Amplifiers," Doctor of Philosophy, School of Technology, Oxford Brooks University, 2004.

[13] R. Wu, F. J. Lidgey, and K. Hayatelh, "Design of differential amplifier with negative impedance compensation," presented at the IEEE International Conference on Circuits & Systems for Communications, Shanghai, 26th-28th May 2008.

[14] M. T. Ali, R. Wu, P. Callaghan and P Rapajic, "Experimental Study of a Highly Linear Amplifier Using Negative Impedance Compensation Technique," presented at the IET Active RF Devices, Circuits and Systems Seminar, Belfast, UK, 2011.

[15] P. B. Kenington, High-Linearity RF Amplifier Design. London: Artech House, 2000.

[16] P. E. Allen and D. R. Holberg, CMOS Analog Circuit Design: Oxford University Press, 2002.