# FH-SS DDS-PLL based Frequency Synthesizer

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***Abstract*—A scheme of frequency hopping spread spectrum (FH-SS) frequency synthesizer suitable for synthesis of radio-frequency (RF) carrier signal in very high frequency (VHF) band is proposed, implemented and tested. The synthesizer is based on the direct digital frequency synthesis (DDFS or DDS) and phase locked loop (PLL) with dynamic monitoring of varicap's voltage to reduce switching time. The results of measurement confirm high performance of the proposed scheme.**

***Keywords-DDS; PLL; RF carrier; synthesizer***

## I. INTRODUCTION

The synthesis and modulation of RF carrier signal is of paramount importance in radio-communication systems. The performance of the RF carrier signal defines the basic characteristics of the radio-transmitter, such as spectral purity of the output signal, the phase noise of the transmitter, the stability and frequency resolution of the output signal, the bandwidth of the modulated signal around the carrier, etc. So far, several techniques for frequency synthesis of the RF carrier signal have been proposed and used. The most commonly used technique is the frequency synthesis based on the phase locked loop (PLL) [1]. The advantage of the PLL based frequency synthesizer reflects in its simplicity and relatively low-cost components built in it, and rather wide range of frequencies that is capable to generate. The PLL based frequency synthesizer can suppress spurious signals more than 80 dBc. The main disadvantages are inability to achieve high resolution of the output frequency and longer transition times switching from one frequency to another [1]. Another widely used technique for frequency synthesis is direct digital frequency synthesis (DDFS or DDS) [2], [3]. Due to its properties, alone or in combination with PLL, DDS is increasingly being used in modern radio-communication systems [4-6]. DDS based frequency synthesizers have a high resolution of the output frequency, very short switching time, low phase noise, a large ratio of minimal and maximal output frequency, the ability to perform digital modulation of frequency, phase, and amplitude (FSK, PSK, ASK), the continuous (linear) sweep of the output frequency, the quadrature signal generation, etc [7]. In addition to the limited maximal output frequency, DDS based frequency synthesizers have a higher level of spurious signals in the spectrum of the output signal in comparison to the PLL based frequency synthesizers. This represents a major holdback in means of DDS direct application in the RF carrier signal generation. The present level of wideband spurious-free dynamic range (SFDR) in the spectrum of the DDS output signal is near 50-60 dBc, while narrowband SFDR is greater than 80 dBc [7]. The level of DDS wideband SFDR is inappropriate for DDS to be used in most RF applications. It is especially expressed in the case of radio-transmitters employing angle modulation. Here, nonlinear amplifiers are used to produce high output power, thus degrading the SFDR by amplifying the low-level spurious signals close to the RF carrier. Therefore, DDS based frequency synthesizers must have excellent wideband and narrowband SFDR in order to be used as exciters to the chain of nonlinear amplifiers. To combine advantages of aforementioned techniques, a hybrid DDS-PLL based frequency synthesizer in very high frequency (VHF) band suitable for FH-SS radio is proposed, implemented, and tested.

The remainder of this paper is organized as follows: In Section 2, the block scheme of hybrid synthesizer for the frequency synthesis of RF carrier signal in FH-SS radio is proposed and described. Results of measurement are given in Section 3, while conclusion remarks are drawn in Section 4.

## II. THE PROPOSED HYBRID SCHEME

The block scheme of proposed hybrid FH-SS VHF frequency synthesizer is depicted in Fig.1.

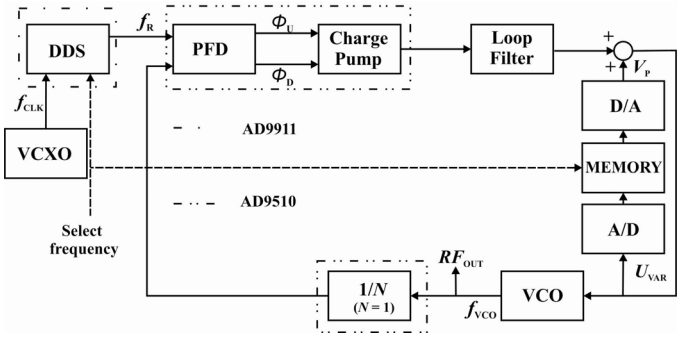


Figure 1. DDS-PLL based frequency synthesizer

The scheme uses unitary PLL without multiplication of reference frequency $f_R$ ($N$ = 1, where $N$ is a factor of multiplication or PLL feedback division factor) and DDS to produce the reference frequency. PLL output frequency $f_{VCO}$ is equal to the reference frequency $f_R$, thus PLL behaves similar to narrowband filter with the central frequency set to the reference frequency $f_R$. The PLL parameters (natural frequency $\omega_n = 2\pi f_n$ and damping factor $\xi$) determine passband

bandwidth of the PLL. PLL will suppress spurious signals in the spectrum of the voltage-controlled oscillator (VCO) output signal if the spurs are out of the PLL bandwidth. This way, wideband spurs present in the DDS driven PLL reference signal will be suppressed. Thus, PLL improves SFDR of DDS and makes it suitable for role of transmitter exciter in RF applications.

In the proposed scheme, the output frequency $f_{VCO}$ is equal to the reference frequency $f_R$, and the problem of suppressing spectral components at frequencies $f_{VCO} \pm n \cdot f_R$, $n = 1, 2, 3,\ldots$ comes down to output signal harmonics filtering, which is not the case with traditional integer-division and non-integer-division based frequency synthesizers. Change of the output frequency $f_{VCO}$ is done by changing the DDS output frequency $f_R$, resulting in high frequency resolution of the output signal equal to the frequency resolution provided by the DDS. Further, since the used PLL is unitary, the phase noise of the output signal is equal to the DDS phase noise increased for noise produced by phase-frequency detector (PFD), charge pump, loop filter and power supply. Outside the PLL bandwidth, the phase noise of the VCO is dominant. DDS has relatively low phase noise and with careful choice of PLL components, low phase noise of the output signal can be achieved. In the case of the reference signal multiplication, the phase noise is increased for factor of $20 \cdot \log N$. Therefore, the phase noise of the output signal does not increase additionally using the unitary PLL. It is especially important for electromagnetic compatibility (EMC) among radio equipment.

The parameters $\omega_n$ and $\xi$ for the second order unitary PLL and passive filter are determined using expressions [8]:

$$\omega_n = \sqrt{\frac{K_0 I_p}{2\pi C}}, \quad \xi = \frac{RC}{2}\sqrt{\frac{K_0 I_p}{2\pi C}}, \qquad (1)$$

where $K_0$ denotes VCO gain ($K_0$ radians/second/volt) and $I_p$ is the charge pump current ($I_p$ ampere). The above expressions (1) show that $\omega_n$ and $\xi$ can be maintained constant within PLL's operating range without the need of external compensation, if $K_0$, $I_p$, $R$ and $C$ do not change. This results in steady behavior of the PLL in terms of noise and transient regimes. The choice of $\omega_n$ and $\xi$ is a compromise between mutually opposite conditions. Greater $\omega_n$ provides greater bandwidth or shorter switching time of the PLL, while lower $\omega_n$ gives better performance in terms of SFDR.

Relatively high reference frequency $f_R$ allows greater natural frequency $\omega_n$. PLL lock-time equals $T_s = -\ln((f_e/\Delta f)\cdot(1-\xi^2)^{1/2})/(\xi\omega_n)$, where $f_e$ denotes acceptable frequency error, $\Delta f$ initial frequency error or initial frequency mismatch [9]. Using the voltage bias $V_P$, a small initial frequency mismatch can be made allowing the PLL with the high natural frequency $\omega_n$ to quickly reduce initial frequency error $\Delta f$ to acceptable error $f_e$. E.g. for $\Delta f$ = 100 KHz, $f_e$ = 100 Hz, $\xi$ = 0.707 and $f_n$ = 500 KHz, PLL lock-time is $T_s$ = 2.23 µs. Bias voltage $V_P$ is produced in the feedback using A/D converter, memory and D/A converter. Voltage-frequency characteristic of the VCO is stored into memory. When new frequency is selected corresponding varicap voltage $V_P$ is read from the memory setting the VCO output frequency close to the selected one. PLL removes remaining phase difference. This way, a very fast change of the PLL output frequency is acquired, which is especially important in fast FH-SS systems. Furthermore, corrections of the varicap voltage $V_P$ are made in stationary regime of the PLL mainly due to temperature variations.

## III. THE RESULTS OF MEASUREMENT

The implemented configuration of the proposed hybrid frequency synthesizer, shown in Fig. 1, used DDS AD9911 chip [7]. As VCXO, crystal with fundamental mode frequency of 10.7 MHz is used [10]. DDS internal PLL uses multiplication factor of 20 to multiply driving VCXO clock frequency $f_{CLK}$ from which the reference frequency $f_R$ is now produced. Phase frequency detector and charge pump are parts of the chip AD9510 [11]. VCO operates in VHF band (30-88 MHz). Loop filter is implemented as first-order passive RC filter. A/D converter, memory and D/A converter are ready-made circuits.

PLL reference signal (i.e. DDS output signal) and PLL output signal are depicted in Fig. 2 (curves 1 and 2, respectively).

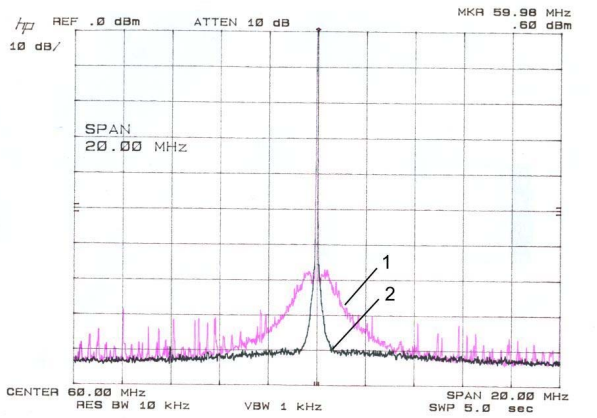


Figure 2. Signal at the output of DDS (curve 1) and at the output of PLL (curve 2) in case of non-modulated RF carrier

PLL improves wideband SFDR of the used DDS and reduces it below -90 dBc for the PLL bandwidth of 100 KHz ($B_{PLL}$ = 100 KHz), as shown on Fig. 2. Spectral components within PLL bandwidth will be present in the spectrum of the VCO output signal, so, narrowband SFDR is defined by the used DDS (for AD9911 it is below -81 dBc in 1 MHz frequency range [7]). Phase noise of the PLL output signal is shown in Fig. 3 and Fig. 4.

Values obtained from Fig. 3 and Fig. 4 reduced by $10 \cdot \log$(RES BW), where RES BW is HP8568B spectrum analyzer resolution bandwidth, are given in Table I.

TABLE I. PHASE NOISE OF PLL'S OUTPUT SIGNAL

| | @ | | | |
|---|---|---|---|---|
| | 1 KHz | 10 KHz | 100 KHz | 1 MHz |
| Phase noise (dBc/Hz) | -100 | -107 | -110 | -140 |

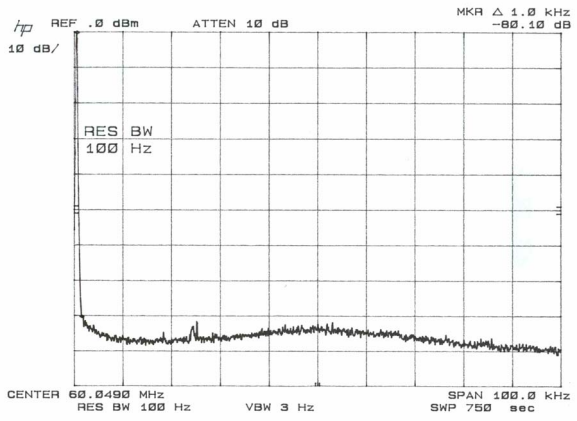


Figure 3. PLL phase noise (span = 100 KHz, RES BW = 100 Hz)

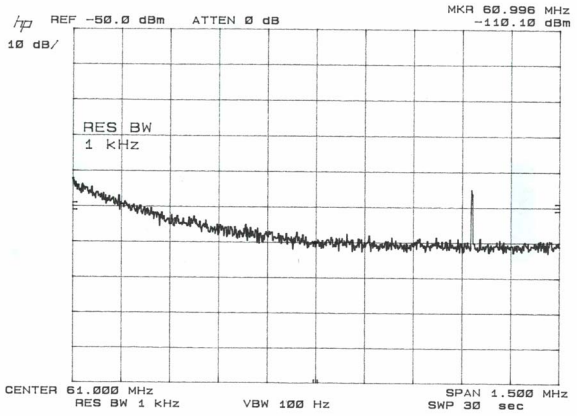


Figure 4. PLL phase noise (span = 1.5 MHz, RES BW = 1 KHz)

The proposed hybrid frequency synthesizer with the measured and calculated phase noise, narrowband and wideband SFDR is suitable for most RF applications.

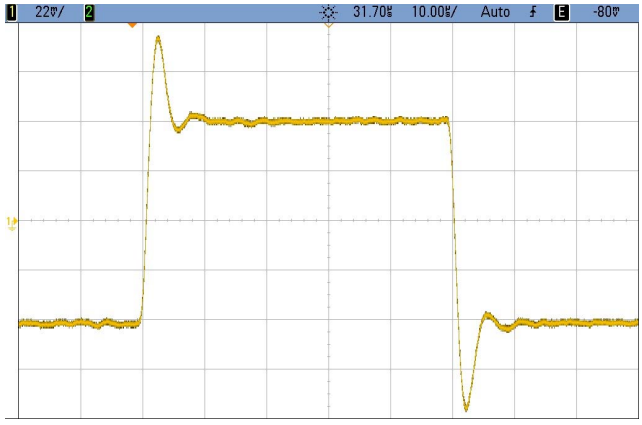


Figure 5. PLL lock-time; $\Delta f$ = 100 KHz, $f_n$ = 200 KHz and $\xi \approx 0.7$

PLL lock-time for initial frequency error $\Delta f$ = 100 KHz and parameters of the PLL $\xi \approx 0.7$, $f_n$ = 200 KHz is shown in Fig. 5. For given values lock-time is within 10 µs, while for the acceptable error $f_e$ = 100 Hz equals $T_s$ = 8.165 µs.

Using the bias voltage $V_P$, it is possible to reduce the frequency error within 10 KHz ($\Delta f = |f_{VCO} - f_R| \leq 10$ KHz), setting the lock-time to $T_s$ = 5.574 µs for $f_e$ = 100 Hz, $\xi \approx 0.7$ and $f_n$ = 200 KHz.

## IV. CONCLUSIONS

A method for the frequency synthesis of RF carrier signal in VHF band suitable for FH-SS radio is proposed, implemented and tested. Results of measurement confirm high performance of the proposed method. Low spurious signals, low phase noise, and high frequency resolution of the output signal make it suitable for most RF applications. RF carrier frequency acquired by using proposed method, has better performances than signal generated either by DDS or by PLL. With relatively high natural frequency of PLL combined with VCO bias voltage, it is possible to obtain short switching time, which is necessary for fast FH-SS radio. Finally, the proposed hybrid scheme can be applied beyond operating range covered by the DDS. With the fixed division factor ($N > 1$) in the feedback of the PLL, extended frequency range can be covered with a cost of certain degradation of some performance measures.

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