Operational Transconductance Amplifier in 350nm CMOS technology

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***Abstract*— This paper presents transistor level design of operational transconductance amplifier in CMOS technology. Custom designed, circuit is to be built-in into the mixed-signal, switched capacitor circuit. Amplifier targets relatively high slew-rate and moderate open loop gain with megahertz order gain-bandwidth. Adopted architecture is discussed appreciating application in switched capacitor circuits. Circuit behavior is examined through set of simulations. Obtained results confirmed desired behavior. Target technology process is TSMC 350nm.**

Keywords-Integrated circuit; Amplifier; Switched capacitor circuits; CMOS technology

I. INTRODUCTION

Operational Transconductance Amplifier (OTA) is considered to be the very fundamental part of analog integrated circuits (IC). Almost every on-chip active block for analog signal conditioning is built on top of it. Concerning this fact switched capacitor (SC) circuits are not exception. Design covered in this work is meant to be embedded into analog part of the second order ΔΣ analog-to-digital converter (ADC) discussed in [1]. Since ADC consists of SC circuits there is inherent request for relatively high slew-rate and gain-bandwidth. As shown in [2], open loop i.e. DC, gain has the smallest influence on SC circuit characteristics therefore moderate open loop gain is sufficient. Table I summarizes main OTA design parameters set by the higher order circuit requirements.

TABLE I. TARGET OTA PARAMETERS

Parameter	*Description*	*Value*
A_0	DC, open loop, gain	> 50 dB
f_{gbw}	Gain-bandwidth	> 120 MHz
SLR	Slew rate	> 120 V/μs

Parameters like, input/output dynamic range (DR), common mode (CMRR) and power supply (PSRR) rejection ratios should be as large as possible. Since TSMC 350nm technology process supports relatively high, 3.3V, power supply voltage this requirements are expected to be fulfilled.

Circuit supposed to be fully differential which implies utilizing some form of common mode feedback (CMFB) circuitry. Also OTA has to have its own bias point generator in order to provide appropriate transistor operation. Since on-chip capacitors are considered, 2pF differential load capacitance is adopted. This value is also set by higher order circuit requirements concerning *kT*/*C* noise of ΔΣ structure explained in [2]. It should be mentioned that target technology process offers Poly-insulator-Poly (PiP) capacitors with 864 aF/μm^2 capacitance per unit area. Hence the value of 2 pF for load capacitance gives reasonably high capacitor area of 2314.81 μm^2 (48.11μm x 48.11μm).

Paper is organized as follows. In second section adopted OTA architecture will be briefly discussed and appropriate subsections will cover circuitry in more details. Third section presents simulation results. Finally, in the fourth section, educative conclusions are drawn and possible improvements are discussed.

II. OTA ARCHITECTURE

Although folded cascode (FC) architecture is commonly adopted for building SC circuits; telescopic architecture is chosen for OTA design in this case. Some related work supporting this idea is published in [3],[4]. It is well known that FC provides wider input common mode range, better input-output common mode relation and high input/output swing [5]. All those advantages imply higher power consumption, lower gain, higher noise and, most importantly in this case, lower speed (i.e. slew-rate and gain-bandwidth). Choosing telescopic architecture means stricter constraint on input/output common-mode voltage choice. Transistor level schematic of OTA with bias and CMFB circuitry is depicted in Fig. 1. Dimensions of all transistors are summarized in Table II. Design can be partitioned in three sub-blocks namely: Core, CMFB and Bias.

A. Core

Transistors M0-M8 are the core of the design. Analyzing structure utilizing simplified model open loop gain is:

$$A_0 \approx g_{m1,2}(g_{m3,4}r_{03,4}r_{01,2} \parallel g_{m5,6}r_{05,6}r_{07,8}). \qquad (1)$$

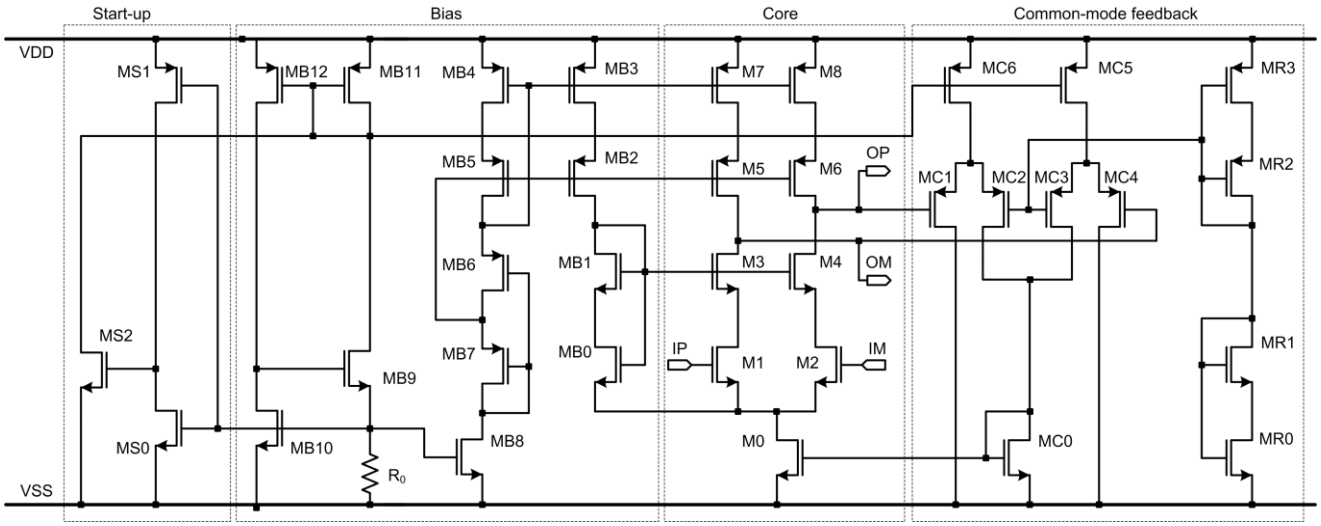

Figure 1. Telscopic OTA with bias and CMFB circuitry

TABLE II. TRANSISTOR DIMENSIONS

Transistors	width/length [µm/µm]
(M1, M2, M3, M4),(M0, M5, M6, M7, M8)	(128/0.8), (256/0.8)
(MB1, MB8), (MB2, MB3, MB4, MB5, MB7, MB10, MB9),(MB11, MB12), MB0,MB6, MS0, (MS1, MS2)	(128/0.8), (256/0.8), (512/0.8), 24/0.8, 88/0.8, 400/0.8, (4/0.8)
(MC0, MC1, MC2, MC3, MC4), (MC5, MC6)	(6.4/0.8), (12.8/0.8)
(MR1, MR3), MR2, MR0	(2.4/0.8), 7.2/0.8, 0.8/0.8

Cascode configuration by itself provides sufficient DC gain and (1) is expected to meet the DC gain requirements. Being single stage, there is no need for frequency compensation. Stability is also guaranteed by relatively large, 2pF differential load capacitance, C_L. Therefore gain-bandwidth is mainly determined by transconducatance of amplifying devices, $g_{m1,2}$, and load capacitance ratio. Design procedure is as follows. Transconductance of M1 and M2 devices should satisfy the following equality:

$$g_{m1,2} = 2\pi f_{gbw} C_L . \qquad (2)$$

For given gain-bandwidth and load capacitance, g_m equals to about 1.5mS. Taking into account fully differential case this value is doubled. In order to properly size amplifying devices, characteristics shown in Fig. 2, 3 and 4 are addressed. All those curves are extracted using SPICE [6]. Fig. 2 shows composite figure of merit i.e. unity current gain frequency, f_t, and transistor efficiency, g_m/I_D, product versus overdrive voltage, $V_{ov}=V_{GS} - V_{TH}$. Observing these curves for different channel lengths one can find optimum bias point which compromises between speed and efficiency. This value is about 200mV.

Knowing this, the channel current can be extracted. Namely, for overdrive voltage of 200mV Fig. 3 indicates the efficiency of about $10V^{-1}$ which gives the channel current I_D= 300µA.

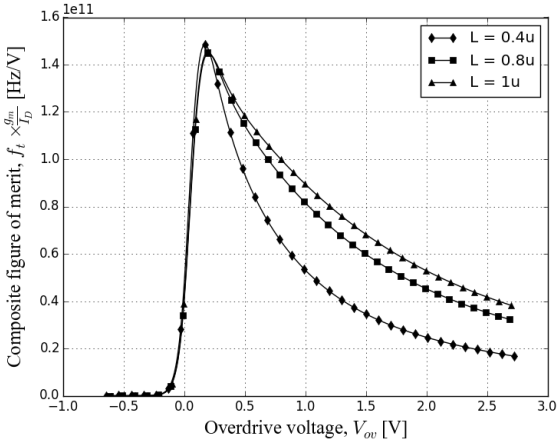

Figure 2. Composite figure of merit versus overdrive voltage

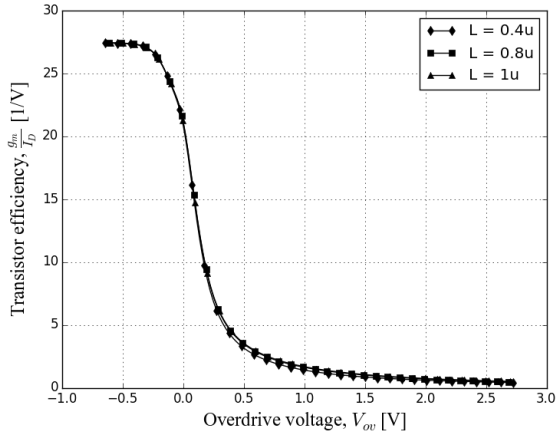

Figure 3. Transistor efficiency versus overdrive voltage

To pick suitable channel length one should observe Fig. 4 which shows small signal gain, a_{v0}, versus drain-source voltage of the MOS device in target technology for different channel lengths. It is notable that shorter channel lengths give relatively constant a_{v0} in wide dynamic range. On the other hand a_{v0} reduces significantly as length decrees. It is obvious that there is a tradeoff between dynamic range and gain.

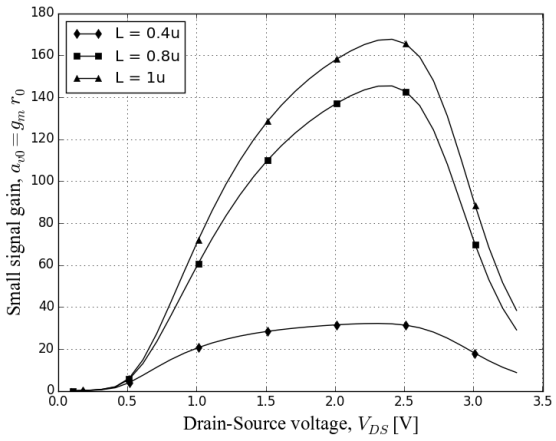

Figure 4. Samll signal gain versus drain-source voltage

If (1) is heavily approximated assuming equal transconductances/resistances, A_0 reduces to $(g_m r_0)^2 = a_{v0}^2$. Picking the L= 0.4μm gives a_{v0} no lower than 20 times in reasonably high dynamic range i.e. 1-3V. Therefore the total gain would be $A_0 \approx 400$ or roughly 52dB. After this value is adopted as good enough the following should be appreciated. Firstly, (1) is heavily approximated and secondly short channel effect is always present. Therefore to mitigate short channel effects, and to ensure gain higher than 50dBs, L= 0.8μm is adopted.

It is also estimated, again using SPICE, that there is a 3.75 μA drain current per 1μm of channel width for chosen channel length in target technology. Accordingly, for 300μA current the minimal width of amplifying devices is W= 80 μm resulting with width-length ratio of 100. This value sets the initial dimensions and the dimensions of all other transistors are drawn based on it. Eventually, final dimensions end up being larger in order to fully meet requirements given in Table I.

B. Common Mode Feedback

CMFB circuitry in Fig. 1 consists of transistors MC0-MC6. Circuit is realized as differential structure which serves as detector of output common-mode voltage change. Ideally circuit should stay inactive in presence of differential output signal. In combination with core transistor M0 negative feedback is formed.

Circuit operation can be qualitatively explained as follows. Suppose there is a positive increment in output common-mode voltage i.e. gate potential of transistors MC1 and MC4 is increased. This will cause reduction of MC1/4 drain currents. Consequently currents of transistors MC2 and MC3 will increase since constant current is forced through MC5/6 and gate of MC2/3 is tied to fixed potential. To ensure maximum output swing, this potential is set to $V_{DD}/2$ by appropriate sizing of MR0-MR3. Because sum of MC2 and MC3 currents flows into MC0 its gate-source voltage, will increase as well. Since core transistor M0 practically represents common-source stage in this signal path, the drain voltage of M0 will decrease. Finally this voltage drop propagates to the output through common-gate structure M1,2/3,4 opposing the initial common-mode voltage increase. Similarly, for differential change at the OTA output, current through MC0 remains unchanged hence, ideally, there is no feedback reaction. Amount of negative reaction is trimmed by MC0/M0 dimensions ratio. To avoid potential unwanted positive feedback reaction through MC5/6, M7/8/5/6 path, MC5/6 and M7/8 transistors are biased from different points.

It is obvious that CMFB loads OTA core degrading dynamic characteristics. Therefore dimensions of CMFB transistors are kept as small as possible. As OTA is to be built into SC circuit, it is likely that this part of the design will be replaced with active CMFB SC network [7]. This way power consumption will be significantly reduced.

C. Bias

Bias circuit is composed of transistors denoted as MB0-MB12 in Fig. 1. Reference current is generated using supply independent, self biased, V_{TH} reference. This reference uses the fact that sensitivity of the active device voltage to the power supply change is always less than unity. This is governed by square root relation between transistors overdrive voltage and drain current. When circuitry is arranged to generate current of active device by its own overdrive voltage, it results with independent voltage reference for power supply. In this case it is done with transistors MB9-MB12 and resistor, R_0. Practically current generated at the gate of MB10 transistor is mirrored back into its drain current thorough MB11/12 current mirror. Consequently it is important to determine appropriate value of R_0 resistance.

From one side current, I_0, in MB9/11 branch is limited by resistor R_0. On the other hand the very same current sets MB10 overdrive voltage. Therefore equation (3) holds. All values in (3) are referred to transistor MB10.

$$I_0 R_0 = V_{TH} + \sqrt{\frac{2I_0}{k'(W/L)}}. \qquad (3)$$

Here k' is intrinsic MOSFET transconductance i.e. mobility and gate oxide capacitance pre unity area product, $\mu_0 C'_{ox}$. Solving (3) by R_0, and appreciating relation $g_m^2 = 2k'(W/L)I_0$ (4) arises.

$$R_0 = \frac{V_{TH}}{I_0} + \frac{2}{g_m}. \qquad (4)$$

Choosing I_0= 600μA (tail source M0), g_m = 6mS (assuming relatively constant overdrive voltage of M0/MB10) and

knowing that V_{TH} for NMOS device in target technology is about 0.78V, it comes that the value for R_0 is 1.63kΩ. This value is reduced to 1.2kΩ trading power consumption for better dynamics.

Since the reference voltage is self-biased there is a need for start-up circuit to prevent zero current state. Start up circuit is designed with transistors MS0-MS2. If there is a zero current in the circuit the voltage at R_0 is low. This low state feeds the MS0/1 inverter which turns on MS2 and providing the low potential at the gates of PMOS MB11/12. This condition opens the path for the current to flow from power supply towards R_0. Consequently, voltage at the MB10 gate increases. Inverter triggers once again turning the MS2 off. It is important to emphasis that size of the MS0 should be much greater then size of MS1. This way the overdrive voltage of MS0 is quite small, allowing inverter to trigger with lower voltage then $V_{DD}/2$. This ensures that inverter turns of MS2 which normally should be cutoff.

The reset of the bias circuitry (MB0-MB8) serves to distribute generated reference to appropriate points. Transistors MB3-MB5 form high swing cascode current mirror biased with MB6/7 Sooch structure [8]. Transistors MB0/1 are used in similar manner to bias M3/4.

III. SIMULATION RESULTS

Circuit's behavior is examined through set of various simulations in SPICE. Results at room temperature are summarized in Table III.

TABLE III. SIMULATED OTA CHARACTERISTICS

Param.	Description	Condition	Value
A_0	DC, open loop gain	open loop/closed loop[a]	57.6 dB
Φ_M	Phase margin	open loop/closed loop	83 °
f_{GBW}	Gain-bandwidth	open loop	140 MHz
		closed loop	126 MHz
SLR	Slew rate	closed loop, excitation: pulse, ±(*ICMR*/2) V, 100kHz	190 V/μs
t_S	Settling time		16.6 ns
V_{OMAX}	Maximum output swing	closed loop, excitation: sine, ± 3.3 V, 1MHz	± 1.83 V
PSRR	Power supply rejection ratio	open loop, from V_{DD}	215 dB
		open loop, from V_{SS}	218 dB
CMRR	Common-mode rejection ratio	open loop, from V_{CM}	240 dB
ICMR	In. common-mode range	open loop	4 mV
		closed loop	2.54 V
OCMR	Out. common-mode range	open loop	1.92 V
		closed loop	2.74 V

a. Unity gain feedback configuration

As can be seen from Table III, target design requirements concerning open loop gain, gain-bandwidth and slew rate are met. It can be also noted that circuit is slightly overdesigned. This is to leave some margin for PVT (Process, Voltage, Temperature) variations and noise which will inevitable arise at layout/physical level. Good circuit dynamics are paid with burning extra power. Total power of the circuit is quite high and it is estimated to 9.83mW. Again, this value can be significantly reduced by changing the CMFB circuitry as explained in section II. Since fully differential power-supply and common-mode rejection ratios are quite high as expected. Usage of high swing cascodes bias resulted with satisfactory output swing.

Even open loop analysis confirms stability it is of curtail importance to check circuit's closed loop behavior. This is done by using famous Middlebrook method, where instead open loop, total loop gain is examined [9]. Results are graphically presented in Fig 5.

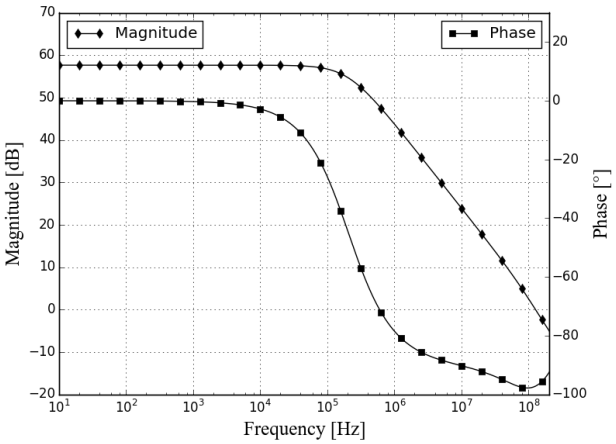

Figure 5. Total loop gain (Magnitude and Phase) versus frequency

This method is considered to be the most trustable when examining stability of feedback systems. It is also favorable because there is no need to break feedback loop hence bias points are not deteriorated. Usually leading CAD vendors, implement this method into its simulation software (e.g. Cadence® Spectre, `iprobe` component in conjunction with `stb` simulation directive). Nevertheless, diving into the [9] one can build its own SPICE deck for implementing the method.

IV. CONCLUSION

This paper presents one design example of OTA circuit considering CMOS 350nm technology process. Designed circuit is to be integral pat of ΔΣ ADC. Adopted architecture is discussed with emphasis on individual sub-blocks namely: Core, Common-Mode Feedback and Bias.

Design procedure of each sub-block is given, as well. For this purpose a set of useful curves is extracted using SPICE giving the insight into MOS device behavior in target technology process. Important design tradeoffs are drawn based on those curves. Transistor level simulation results are presented and discussed. Based on these results one can conclude that circuit meets severe dynamic requirements while preserving stability. Consequently power consumption is increased hence further work will be focused on optimizing design in this direction.

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